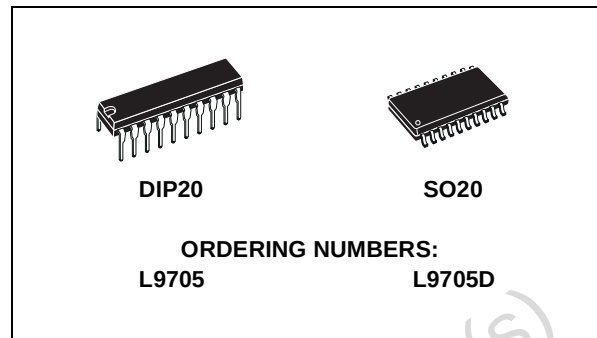


## DOUBLE QUAD CONTACT INTERFACE CIRCUIT

- OPERATING DC SUPPLY VOLTAGE RANGE 5V TO 25V
- SUPPLY OVERVOLTAGE PULSE UP TO 40V
- VERY LOW STAND-BY QUIESCENT CURRENT, MAX 50 $\mu$ A
- INTERNAL CLAMPING DIODES AT CONTACT INPUTS TO  $V_s$  AND gnd WITH PULSE CURRENT CAPABILITY UP TO +50mA, -75mA
- CHIP ENABLE FUNCTION AND TRISTATE OUTPUTS FOR PARALLEL BUS CONNECTION
- NOMINAL CONTACT CURRENTS OF 10mA DEFINED WITH EXTERNAL CONTACT SERIES RESISTORS  $R_{IN1-8}$
- CONTACT STATUS MONITORING BY MEANS OF COMPARING THE RESISTANCE AT CONTACT SENSE INPUTS WITH THE INTERNAL REFERENCE RESISTOR VALUE
- RESISTANCE COMPARING WITH HYSTERESIS FOR HIGH NOISE IMMUNITY AND IMMUNITY TO GROUND AND BATTERY POTENTIAL DIFFERENCES

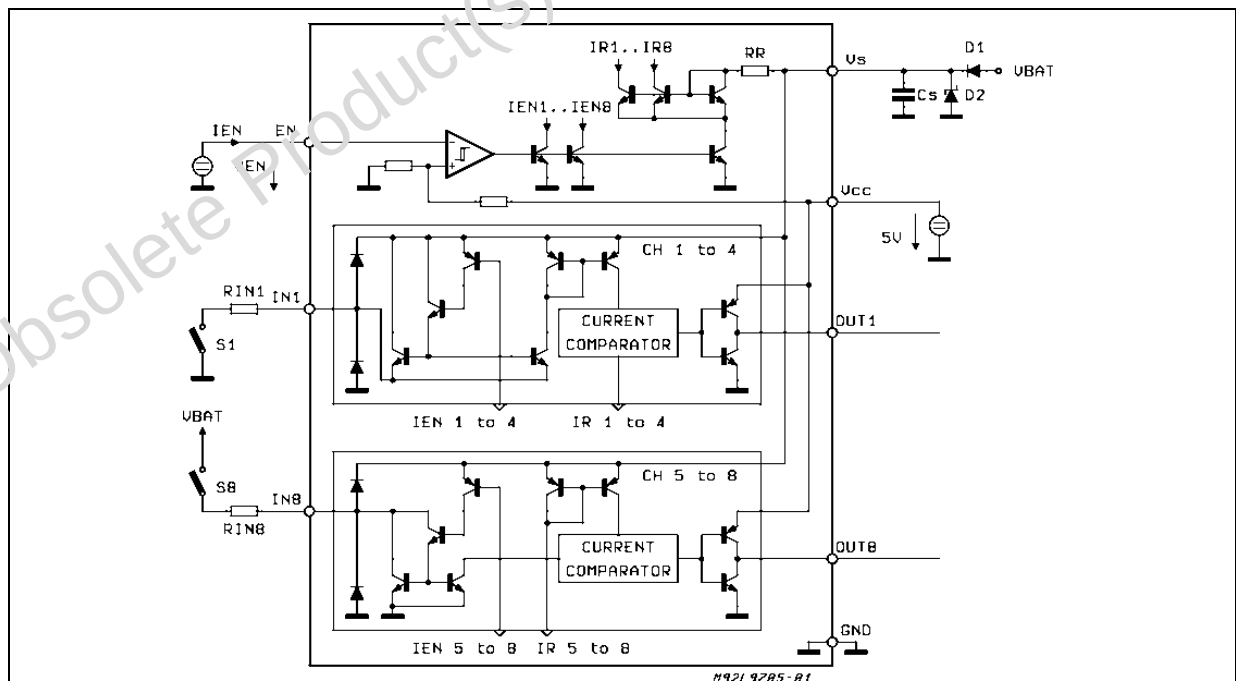


### DESCRIPTION

The L9705 is a bipolar monolithic integrated circuit for monitoring the status of up to four contacts connected to GND and up to four contacts connected to the battery. The contact sense input supply the contact current and perform the contact resistance comparison function.

At the output the contact status is translated into a logical LOW level (contact closed) or logical HIGH level (contact open).

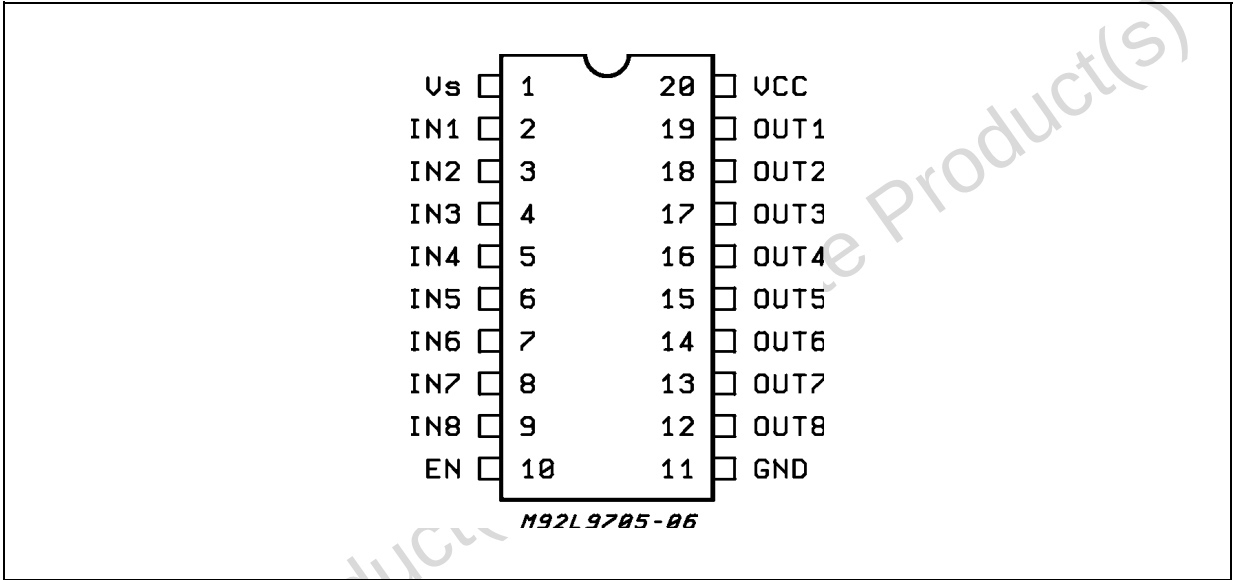
### BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

| Symbol            | Parameter                                                            | Value                                    | Unit     |
|-------------------|----------------------------------------------------------------------|------------------------------------------|----------|
| V <sub>SDC</sub>  | DC Supply Voltage                                                    | +26                                      | V        |
| V <sub>SP</sub>   | Peak Transient Supply Voltage (t ≤ 400ms)                            | +40                                      | V        |
| V <sub>CC</sub>   | Logic Supply Voltage                                                 | 7                                        | V        |
| I <sub>INDC</sub> | Input DC Current                                                     | ±40                                      | mA       |
| I <sub>INP</sub>  | Input Pulse (t <sub>p</sub> = 0 to 2ms; f ≤ 0.2Hz; n = 25000)        | -75 to 50                                | mA       |
| I <sub>OUT</sub>  | Output Current (V <sub>O</sub> = 0 to 5.5V)                          | internally limited                       |          |
| V <sub>EN</sub>   | Enable Input Voltage                                                 | V <sub>CC</sub> +0.3V <sub>i</sub> -0.3V | V        |
| P <sub>tot</sub>  | Total Power Dissipation (T <sub>amb</sub> = 80°C)<br>DIP 20<br>SO 20 | 875<br>420                               | mW<br>mW |
| T <sub>j</sub>    | Junction Temperature Range                                           | max 150                                  | °C       |

PIN CONNECTION (Top view)



THERMAL DATA

| Symbol                | Parameter                              | DIP20 | SO20 | Unit |
|-----------------------|----------------------------------------|-------|------|------|
| R <sub>th j-amb</sub> | Thermal Resistance Junction to ambient | 80    | 165  | °C/W |

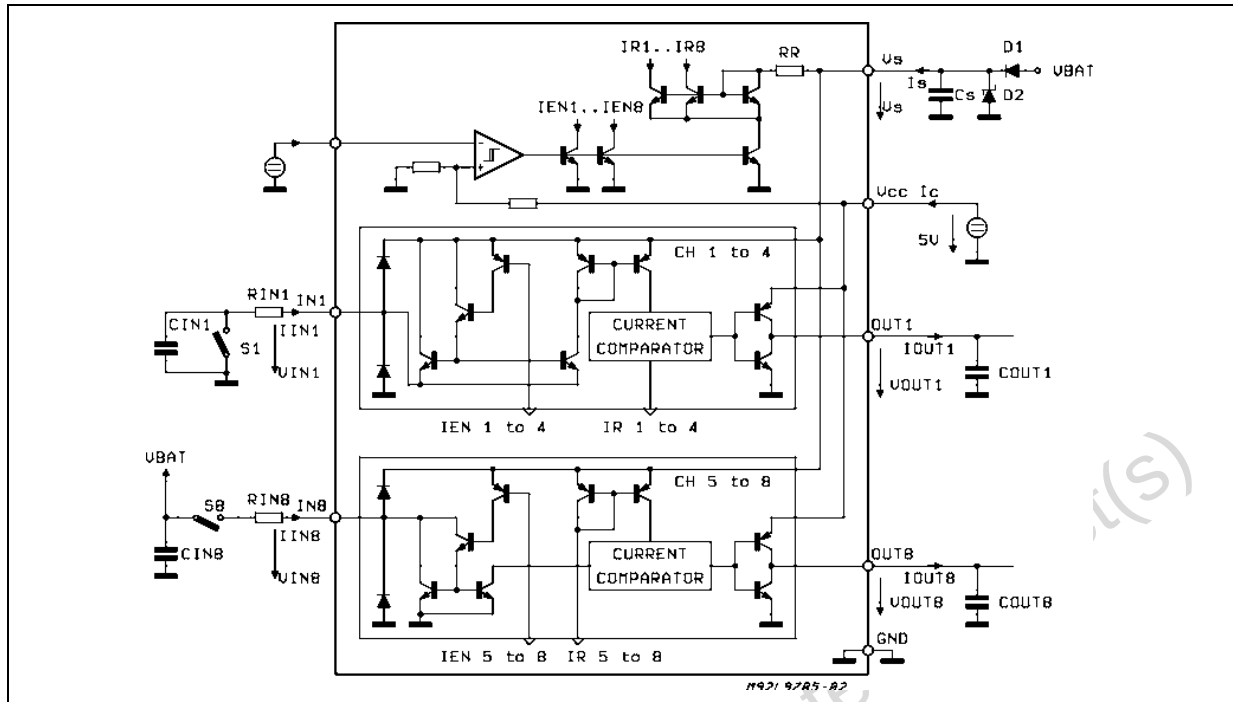
**ELECTRICAL CHARACTERISTICS**

( $V_S = 5$  to  $25V$ ,  $V_{CC} = 4.75$  to  $5.25V$ ,  $V_{bat} - 0.5V < V_S < V_{bat} - 1V$ ,  $T_j = -40$  to  $150^\circ C$  unless otherwise specified.)

| Symbol              | Parameter                                                 | Test Condition                                                                          | Min.              | Typ.            | Max.                           | Unit               |
|---------------------|-----------------------------------------------------------|-----------------------------------------------------------------------------------------|-------------------|-----------------|--------------------------------|--------------------|
| $V_{ENL}$           | Enable Input Voltage LOW (device activated)               |                                                                                         | -0.3              |                 | 0.8                            | V                  |
| $V_{ENH}$           | Enable Input Voltage HIGH                                 |                                                                                         | 2.4               |                 | $V_{CC}$                       | V                  |
| $V_{ENh}$           | Enable Input Threshold Hysteresis                         |                                                                                         | 200               | 420             | 800                            | mV                 |
| $I_{EN}$            | Enable Input Current                                      | $2.4V < V_{EN} < V_{CC}$<br>$0V < V_{EN} < 0.8V$                                        | -5                | -1              | 5                              | $\mu A$<br>$\mu A$ |
| $V_{OUTH}$          | Output Voltage HIGH                                       | $0 < I_{OUT} < 100\mu A$                                                                | 4                 | $V_{CC} - 0.1$  | $V_{CC}$                       | V                  |
| $I_{OUT}$           | Output Current                                            | OUT status = HIGH; $V_{OUT} = 0$                                                        |                   | 0.5             | 2                              | mA                 |
| $V_{OUTL}$          | Output Voltage LOW                                        | $I_{OUT} = -1mA$                                                                        | 0.05              | 0.2             | 0.4                            | V                  |
| $I_{OUT}$           | Output Current                                            | OUT status = LOW; $V_{OUT} = 5.5V$                                                      |                   | -5              | -20                            | mA                 |
| $I_{OUT TS}$        | Output Tristate Current                                   | $0 < V_{OUT} < V_{CC}$                                                                  |                   |                 | 0.5                            | $\mu A$            |
| $V_{IN 1,4}$        | Input Voltage (device active)                             | EN = LOW; $R_{IN} = 1K\Omega$                                                           | $V_S - 2$         | $V_S - 1.5$     | $V_S - 0.4$                    | V                  |
| $V_{IN 5,8}$        | Input Voltage (device active)                             | EN = LOW; $R_{IN} = 1K\Omega$                                                           | 0.4               | 1.5             | 2                              | V                  |
| $V_{IN}$            | Input Voltage During Clamp (device disabled)              | EN = HIGH; $I_{IN} = 30mA$<br>$I_{IN} = -30mA$                                          | $V_S + 0.3$<br>-2 | $V_S + 1$<br>-1 | $V_S + 2$<br>-0.3              | V<br>V             |
| $R_{IL 1,4}$        | Input Resistor LOW Threshold (note 1)                     | $5V < V_S < 16V$ ; $ \Delta V_{GND}  \leq 0.1V_S$<br>$ \Delta V_{BAT}  \leq 0.1V_{BAT}$ | 1.8               | 4               |                                | K $\Omega$         |
| $R_{IL 5,8}$        | Input Resistor LOW Threshold (note 1)                     | $5V < V_S < 16V$ ; $ \Delta V_{GND}  \leq 0.1V_S$<br>$ \Delta V_{BAT}  \leq 0.1V_{BAT}$ | 1.8               | 4.8             |                                | K $\Omega$         |
| $R_{IH 1,4}$        | Input Resistor HIGH Threshold (note 1)                    | $5V < V_S < 16V$ ; $ \Delta V_{GND}  \leq 0.1V_S$<br>$ \Delta V_{BAT}  \leq 0.1V_{BAT}$ |                   | 5.3             | 20                             | K $\Omega$         |
| $R_{IH 5,8}$        | Input Resistor HIGH Threshold (note 1)                    | $5V < V_S < 16V$ ; $ \Delta V_{GND}  \leq 0.1V_S$<br>$ \Delta V_{BAT}  \leq 0.1V_{BAT}$ |                   | 6.5             | 29                             | K $\Omega$         |
| $R_{IL}$            | Input Resistor Threshold Ratio (note 1)                   | $5V < V_S < 16V$ ; $ \Delta V_{GND}  \leq 0.1V_S$<br>$ \Delta V_{BAT}  \leq 0.1V_{BAT}$ | 0.65              | 0.75            | 0.85                           |                    |
| $R_{IH}$            | Input Resistor Threshold Ratio (note 1)                   | $5V < V_S < 16V$ ; $ \Delta V_{GND}  \leq 0.1V_S$<br>$ \Delta V_{BAT}  \leq 0.1V_{BAT}$ | 0.65              | 0.75            | 0.85                           |                    |
| $I_{QC}$            | Quiescent Current                                         | EN = HIGH ( $t_{ENH} > 20\mu s$ )<br>$V_S = 5$ to $16V$ ; $T_j = -40$ to $85^\circ C$   |                   | 20              | 40                             | $\mu A$            |
| $I_{QS}$            | Quiescent Current                                         | all contact open                                                                        |                   |                 | 10                             | $\mu A$            |
| $I_{QS}$            | Quiescent Current                                         | all contact closed                                                                      |                   |                 | 35                             | $\mu A$            |
| $\Sigma I_{IN (2)}$ | Quiescent Current                                         | $ \Delta V_{BAT}  \leq 0.1V_{BAT}$                                                      |                   |                 | 25                             | $\mu A$            |
| $I_{QC}$            | Quiescent Current                                         | EN = LOW                                                                                |                   |                 | 5                              | mA                 |
| $I_{QS}$            | Quiescent Current                                         | EN = LOW                                                                                |                   |                 | 8                              | mA                 |
| $t_{do}$            | Delay Time/Output (EN LOW to Output Data Ready) (note 3)  | $C_{OUT} \leq 50pF$                                                                     |                   |                 | 15+<br>3 $R_{IN} \cdot C_{IN}$ | $\mu s$            |
| $t_{dTS}$           | Delay Time/Tristate (EN HIGH to Output Tristate) (note 3) | $C_{OUT} \leq 50pF$                                                                     |                   |                 | 10                             | $\mu s$            |
| $t_{dIO}$           | Delay Time Input-Output (note 3)                          | EN = LOW; $C_{OUT} \leq 50pF$                                                           |                   |                 | 6                              | ms                 |

- Notes: 1. The input resistor threshold value is a resistor value from the IN-pin to ground at which the corresponding output changes its status (fig.4)  
 2.  $\Sigma I_{IN}$  is the sum of the IN5 to IN8 input currents.  
 3. The delay times are defined from the crossing point of 50% initiating signal amplitude to the crossing point of 50% output signal amplitude

Figure 1. Typical application diagram for the L9705 circuit. The current flowing in the arrow direction is assumed positive. The external capacitors CIN and COUT represent the total wiring capacitance at the corresponding pins.



## FUNCTIONAL DESCRIPTION

The L9705 circuit monitors the status of the contacts which are connected through the series external resistors  $R_{IN}$  to the contact sense input pins. The contacts equivalent circuit is supposed to be as shown in fig.2 for GND connected contacts (IN 1 to 4) and as shown in fig. 3 for  $V_{BAT}$  connected contacts (IN 5 to 8).

Figure 2. The contact sense input connection with the contact equivalent circuit for GND connected contacts.

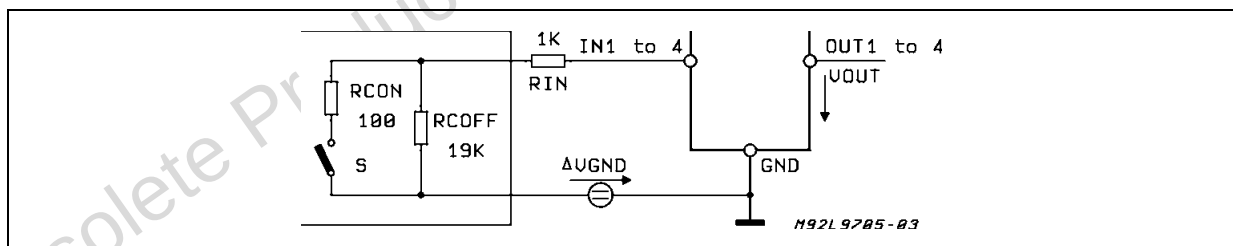
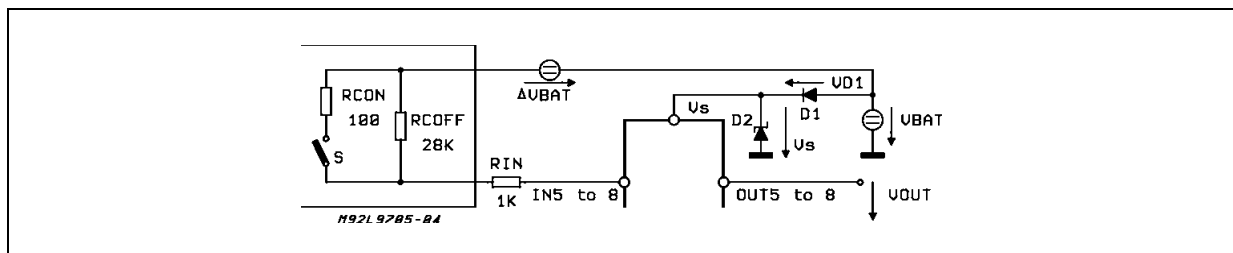


Figure 3. The contact sense input connection with the contact equivalent circuit for  $V_{BAT}$  connected contacts.



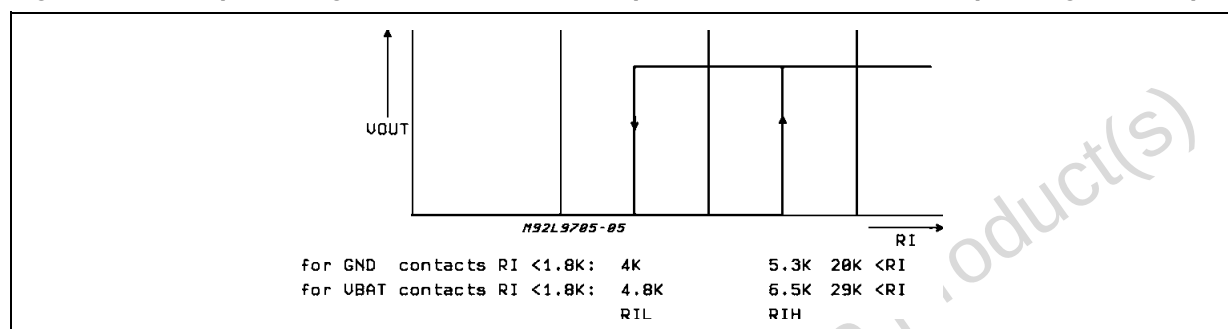
The L9705 circuit compares the input current with the current through the internal reference resistor. The device is designed to work with an external input series resistor of  $R_{IN1-8} = 1k\Omega$ . With this input resistor the contact current, when the contact is closed and the device activated ( $EN = LOW$ ) is:

$$I_{IN} = \frac{V_S - 2V}{1k\Omega}, \text{ for GND contacts, (1)}$$

$$I_{IN} = \frac{V_{BAT} + \Delta V_{BAT} - 2V}{1k\Omega}, \text{ for } V_{BAT} \text{ contacts, (2)}$$

For this calculation the limit value of the  $V_S$  to  $V_{IN}$  and  $V_{IN}$  saturation voltage of 2V was considered so that the lowest limit value of  $I_{IN}$  is calculated in (1) and (2)

**Figure 4. The output voltage as a function of the input resistance at the corresponding sense input.**



The function of the circuit can be demonstrated with the transfer characteristics, showing the output status as a function of the input resistor  $R_I$ , shown in figure 4. The input resistor is a sum of the  $R_{IN}$  and the contact resistance  $R_{CON}$  or  $R_{COFF}$ , for the closed contact:

$$R_I = R_{IN} + R_{CON}, \text{ (3)}$$

and for the open contact:

$$R_I = R_{IN} + R_{COFF}, \text{ (4)}$$

The output goes HIGH when the input resistance increases above 5.3K $\Omega$  (GND contacts) or 6.5K $\Omega$

( $V_{BAT}$  contacts) and goes LOW, when the input resistance decreases below 4K $\Omega$  (GND contacts) or 4.8K $\Omega$  ( $V_{BAT}$  contacts); these values are typical values for the switching thresholds. The limit values of  $R_I = 1.8K\Omega$  (GND contacts) and  $R_I = 1.8K\Omega$  ( $V_{BAT}$  contacts) for LOW and  $R_I = 20K\Omega$  (GND contacts) and 29K $\Omega$  ( $V_{BAT}$  contacts) for HIGH implies that a contact with  $R_{CON} = 100\Omega$  (at  $I_{IN} = 10mA$ ) will be recognized as ON = LOW and a contact with  $R_{COFF} = 19K\Omega$  (GND contacts) or 28K $\Omega$  ( $V_{BAT}$  contact) will be recognized as OFF = HIGH.

These limits are valid within the supply voltage range  $6V \leq V_S \leq 16V$ , the ground potential difference of  $\Delta V_{GND} = 0.1V_S$ , the battery voltage potential difference of  $\Delta V_{BAT} < 0.1V_{BAT}$  and the variation of the reverse battery protection diode D1 voltage from 0.5V to 1V.

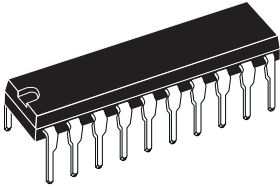
The internal clamping diodes at the contact monitoring inputs together with the external contacts series resistors  $R_{IN}$  allows to withstand the transients at the contact connection. The contact series resistor  $R_{IN}$  limits the input current at the transient.

The dynamic behaviour of the circuit is defined with the times  $t_{do}$  and  $t_{dTS}$ . When the contact is open, the input capacitor  $C_{IN}$  must be charged through the resistor  $R_{IN}$ . In this case the total delay time  $t_{do}$  may be influenced also with the time constant  $R_{IN}C_{IN}$ .

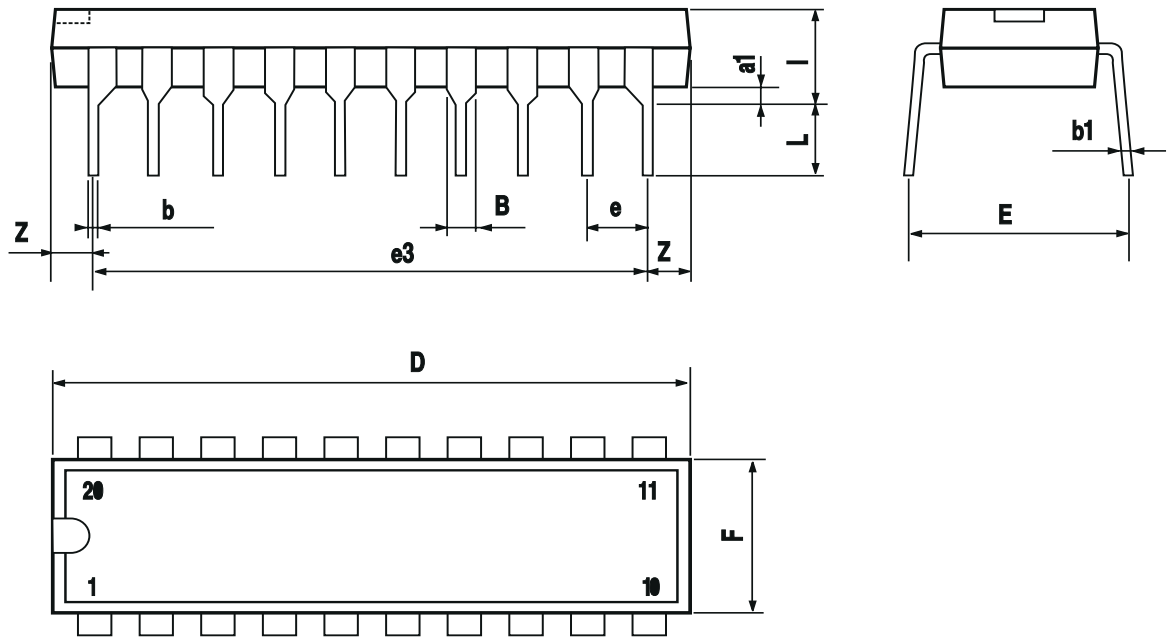
The delay time  $t_{dTS}$ , when disabling the device, is defined only with the internal circuitry. In both cases, output external capacitance less than 50pF is assumed, the internal output capacitance of the tristate buffers are less than 5pF.

| DIM. | mm    |       |      | inch  |       |       |
|------|-------|-------|------|-------|-------|-------|
|      | MIN.  | TYP.  | MAX. | MIN.  | TYP.  | MAX.  |
| a1   | 0.254 |       |      | 0.010 |       |       |
| B    | 1.39  |       | 1.65 | 0.055 |       | 0.065 |
| b    |       | 0.45  |      |       | 0.018 |       |
| b1   |       | 0.25  |      |       | 0.010 |       |
| D    |       |       | 25.4 |       |       | 1.000 |
| E    |       | 8.5   |      |       | 0.335 |       |
| e    |       | 2.54  |      |       | 0.100 |       |
| e3   |       | 22.86 |      |       | 0.900 |       |
| F    |       |       | 7.1  |       |       | 0.280 |
| I    |       |       | 3.93 |       |       | 0.155 |
| L    |       | 3.3   |      |       | 0.130 |       |
| Z    |       |       | 1.34 |       |       | 0.053 |

**OUTLINE AND  
MECHANICAL DATA**



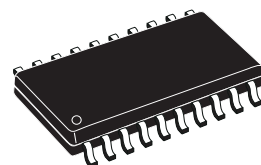
**DIP20**



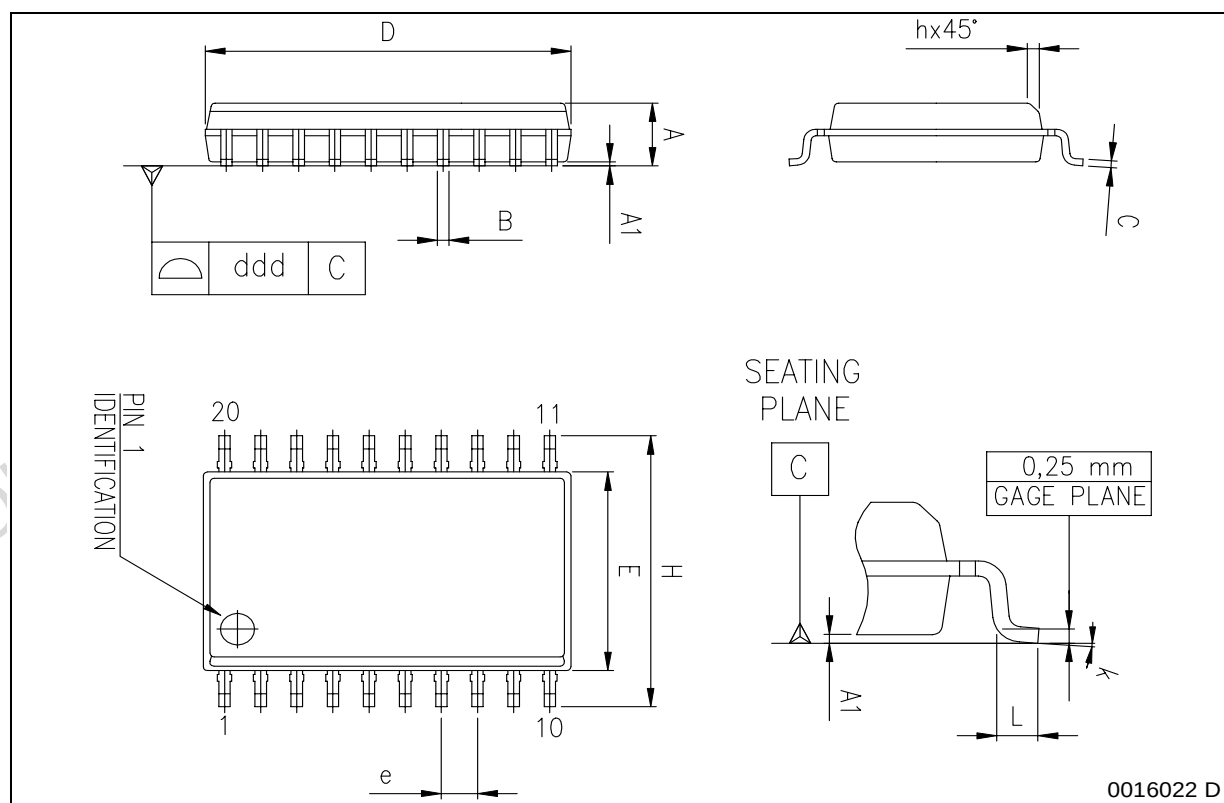
| DIM.             | mm                   |      |       | inch  |       |       |
|------------------|----------------------|------|-------|-------|-------|-------|
|                  | MIN.                 | TYP. | MAX.  | MIN.  | TYP.  | MAX.  |
| A                | 2.35                 |      | 2.65  | 0.093 |       | 0.104 |
| A1               | 0.10                 |      | 0.30  | 0.004 |       | 0.012 |
| B                | 0.33                 |      | 0.51  | 0.013 |       | 0.200 |
| C                | 0.23                 |      | 0.32  | 0.009 |       | 0.013 |
| D <sup>(1)</sup> | 12.60                |      | 13.00 | 0.496 |       | 0.512 |
| E                | 7.40                 |      | 7.60  | 0.291 |       | 0.299 |
| e                |                      | 1.27 |       |       | 0.050 |       |
| H                | 10.0                 |      | 10.65 | 0.394 |       | 0.419 |
| h                | 0.25                 |      | 0.75  | 0.010 |       | 0.030 |
| L                | 0.40                 |      | 1.27  | 0.016 |       | 0.050 |
| k                | 0° (min.), 8° (max.) |      |       |       |       |       |
| ddd              |                      |      | 0.10  |       |       | 0.004 |

(1) "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

## OUTLINE AND MECHANICAL DATA



**SO20**



0016022 D

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics.  
All other names are the property of their respective owners

© 2003 STMicroelectronics - All rights reserved

**STMicroelectronics GROUP OF COMPANIES**

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan -  
Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States  
[www.st.com](http://www.st.com)